P160
Prototype Module
User's Guide

Version 1.1
November 2002

PN# DS-MANUAL-MBEXP2

Memec Design

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1 Overview

The P160 Prototype Module provides a useful expansion, probe, and prototype feature in a small, low cost daughter card form-factor, compatible with any main system board containing the P160 expansion interface. The Spartan-II, Spartan-IIE, Virtex-II and Virtex-II Pro system boards from Memec Design all include the P160 interface and can support the P160 Communications Module. Proper user configuration of the main system board is required to enable the P160 interface and the corresponding expansion module test points. This user guide helps provide the necessary details to develop such a configuration. Complete board schematics are provided in Appendix A for your reference.

2 P160 Prototype Module

The Memec Design P160 Prototype module connects to the main system development board via the P160 I/O module connectors. This board can be used to prototype various user I/O interfaces. A high-level block diagram of this module is given below followed by tables that show the connector pin assignments.

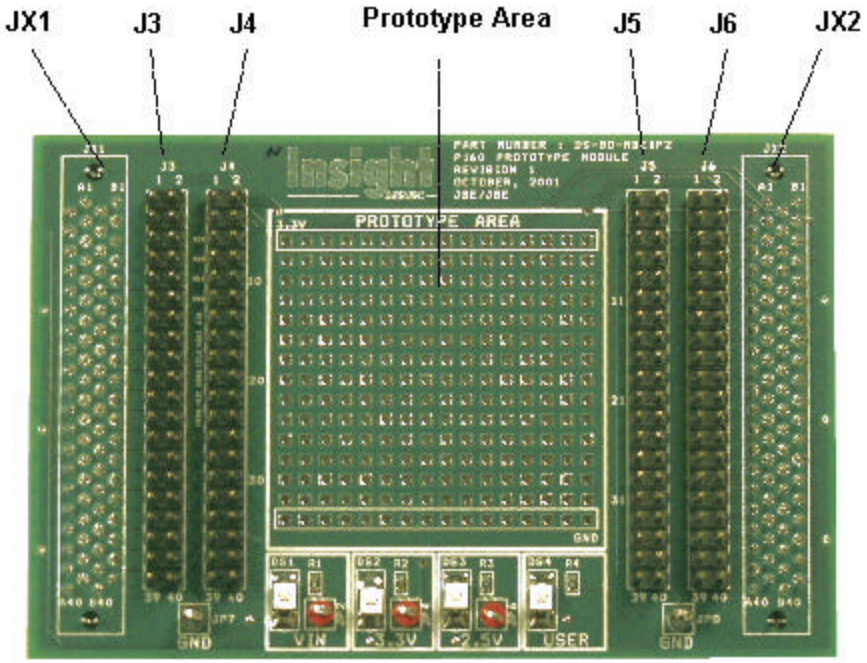


Figure 1– P160 Prototype Module Board

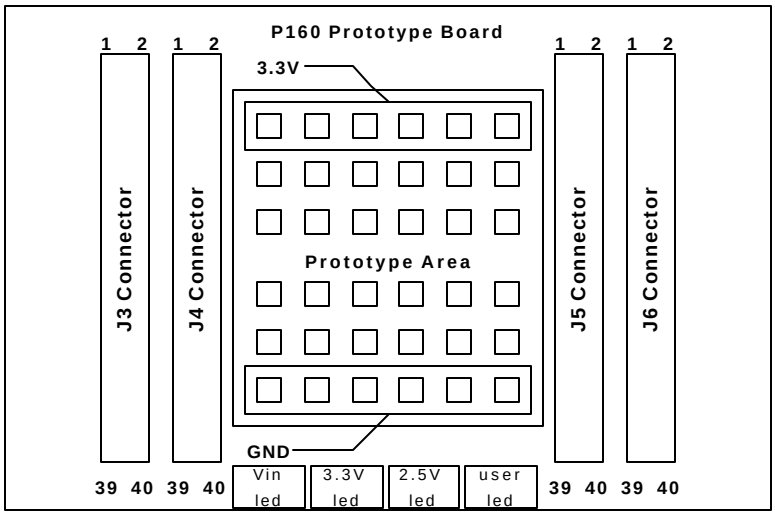


Figure 2 – P160 Prototype Module Block Diagram

3 User Headers

The P160 Prototype module provides four 2 x 20 headers for connection to the P160 Expansion signals. These signals are driven from the main system board and are defined by the FPGA design implemented. Tables 1 through 4 define the connections between the headers and the P160 connectors. Corresponding connections between the P160 connectors and the system board FPGA can be found in the related system board User Guide.

Table 1 – J3 Pin Assignments

FPGA Pin #	J3 Pin #		FPGA Pin #
Vin	1	2	**3.3V**
2.5V	3	4	**GND**
RIOA1	5	6	**NC**
RIOA2	7	8	LIOB8
LIOB9	9	10	LIOB10
LIOB11	11	12	LIOB12
LIOB13	13	14	LIOB14
LIOB15	15	16	LIOB16
LIO17	17	18	LIOB18
LIOB19	19	20	LIOB20
LIOB21	21	22	LIOB22
LIOB23	23	24	LIOB24
LIOB25	25	26	LIOB26
LIOB27	27	28	LIOB28
LIOB29	29	30	LIOB30
LIOB31	31	32	LIOB32
LIOB33	33	34	LIOB34
LIOB35	35	36	LIOB36
LIOB37	37	38	LIOB38
LIOB39	39	40	LIOB40

Table 2 – J4 Pin Assignments

FPGA Pin #	J4 Pin #		FPGA Pin #
Vin	1	2	**3.3V**
2.5V	3	4	RIOB2
TCK	5	6	LIOA9
TDO	7	8	LIOA11
TDI	9	10	LIOA13
TMS	11	12	LIOA15
FPGA.BITSTREAM	13	14	LIOA17
SM.DOUT/BUSY	15	16	LIOA19
FPGA.CCLK	17	18	LIOA21
DONE	19	20	LIOA23
INITn	21	22	LIOA25
PROGRAMn	23	24	LIOA27
GND	25	26	LIOA29
GND	27	28	LIOA31
GND	29	30	LIOA33
GND	31	32	LIOA35
GND	33	34	LIOA37
GND	35	36	LIOA39
GND	37	38	RIOA39
GND	39	40	RIOA40

Table 3 – J5 Pin Assignments

FPGA Pin #	J5 Pin #		FPGA Pin #
Vin	1	2	**3.3V**
2.5V	3	4	RIOB4
NC	5	6	RIOB6
JTAG_LOOPBACK	7	8	RIOB8
JTAG_LOOPBACK	9	10	RIOB10
NC	11	12	RIOB12
NC	13	14	RIOB14
NC	15	16	RIOB16
NC	17	18	RIOB18
NC	19	20	RIOB20
NC	21	22	RIOB22
NC	23	24	RIOB24
GND	25	26	RIOB26
GND	27	28	RIOB28
GND	29	30	RIOB30
GND	31	32	RIOB32
GND	33	34	RIOB34
GND	35	36	RIOB36
GND	37	38	RIOB38
GND	39	40	RIOB40

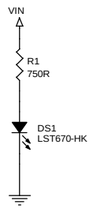
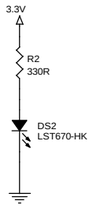
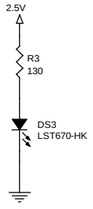
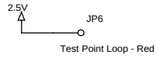
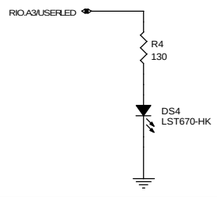
Table 4 – J6 Pin Assignments

FPGA Pin #	J6 Pin #		FPGA Pin #
Vin	1	2	**3.3V**
2.5V	3	4	**GND**
RIOA4	5	6	RIOA3/USERLED
RIOA6	7	8	RIOA5
RIOA8	9	10	RIOA7
RIOA10	11	12	RIOA9
RIOA12	13	14	RIOA11
RIOA14	15	16	RIOA13
RIOA16	17	18	RIOA15
RIOA18	19	20	RIOA17
RIOA20	21	22	RIOA19
RIOA22	23	24	RIOA21
RIOA24	25	26	RIOA23
RIOA26	27	28	RIOA25
RIOA28	29	30	RIOA27
RIOA30	31	32	RIOA29
RIOA32	33	34	RIOA31
RIOA34	35	36	RIOA33
RIOA36	37	38	RIOA35
RIOA38	39	40	RIOA37

Revision History

V1.0	**Initial Release**	**2/13/02**
V1.1	**Update** Minor format updates only	**11/27/02**

Appendix A - P160 Prototype Module Schematics

NAME	LED	TEST LOOP
VIN		
3.3V		
2.5V		
GND		
USER		

V2MB Test module LEDS		
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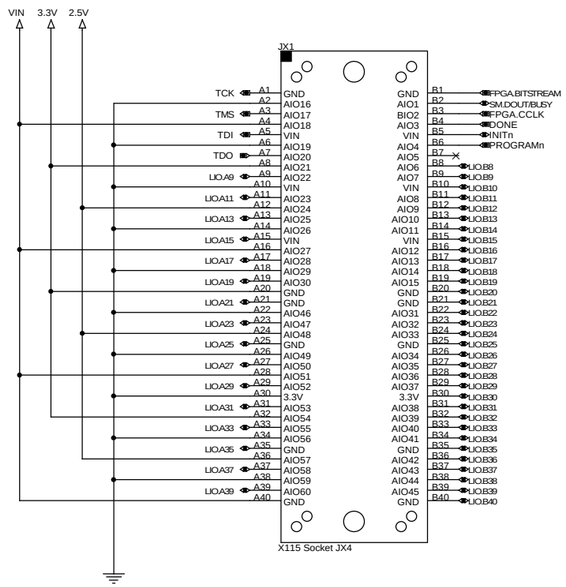
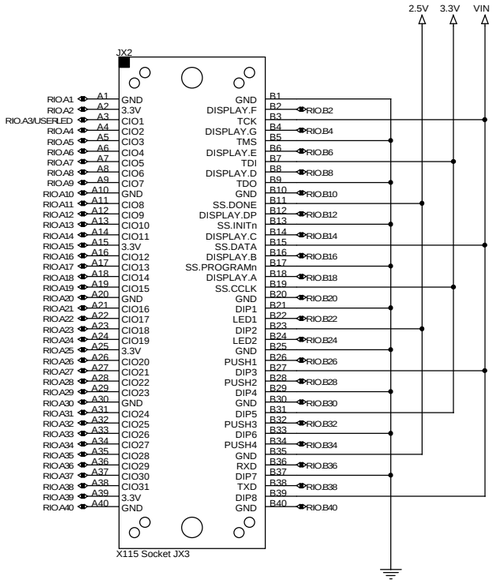
		Size C
		Rev 1
		Designer Jim Elliott
		Sheet 1 of 3



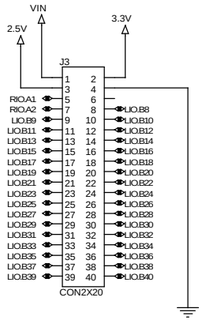


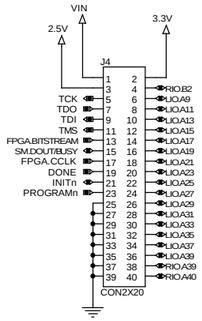
V2MB Test module

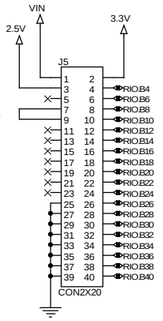
EXPANSION CONNECTORS

MemecBoard
Suite 540, 1212 31st Ave. NE
Calgary, Alberta
Canada
T2E 7S8

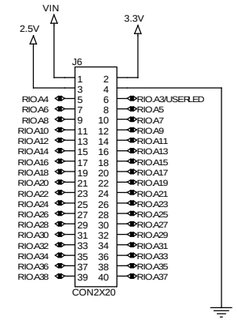
Last Modified	Friday, October 05, 2001
Size	Rev
C	1
Designer	Sheet
Jim Elliott	2 of 3

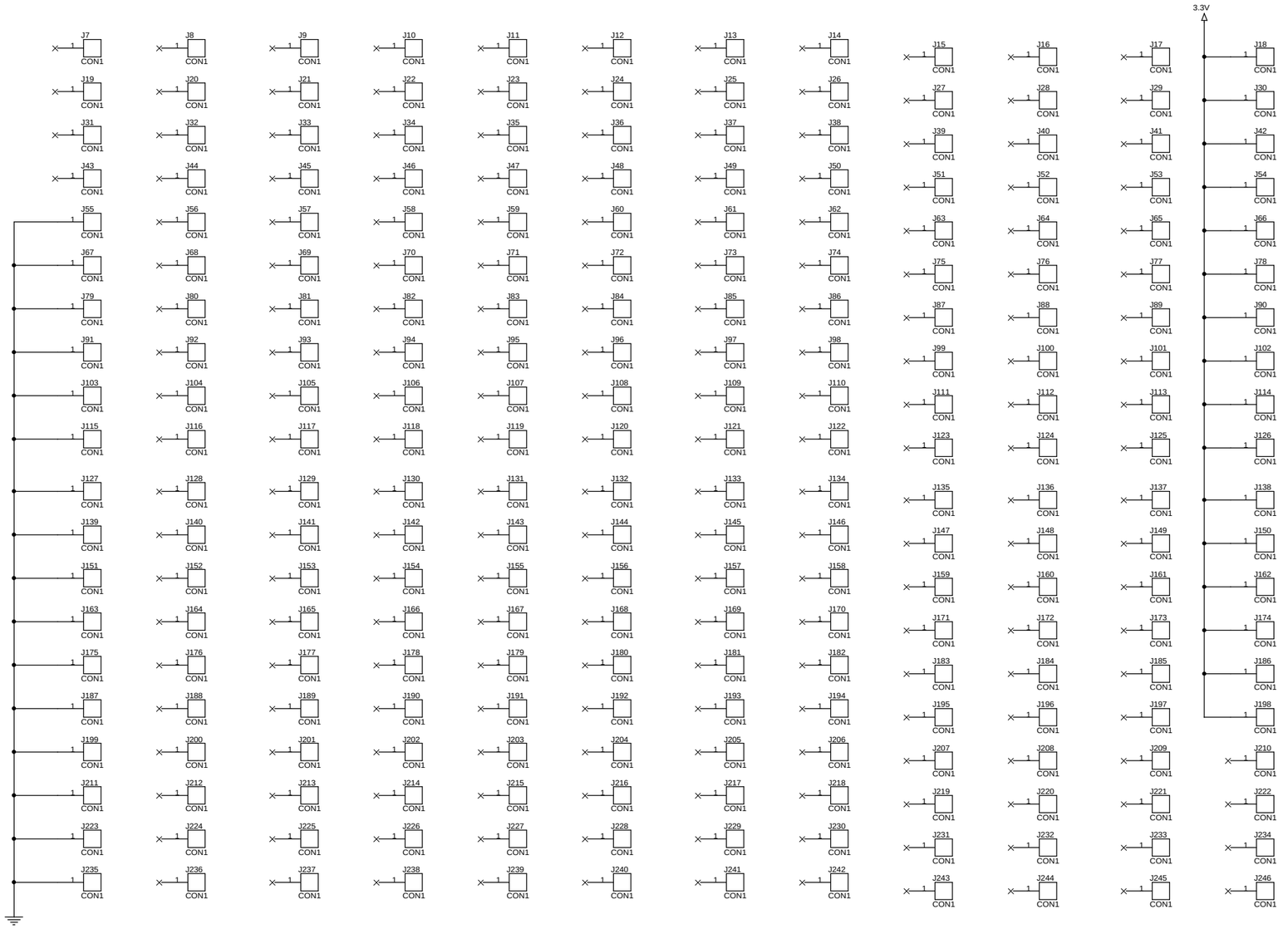






Completes JTAG chain in loopback mode





V2MB Test Module		
HEADERS		
MemecBoard Suite 540, 1212 31st Ave. NE Calgary, Alberta Canada T2E 7S8	Last Modified Friday, October 05, 2001	
	Size C	Rev 1
	Designer Jim Elliott	Sheet 3 of 3